**实验2：**组合逻辑电路实验

一、 实验目的

1、 掌握组合逻辑电路的功能测试。

2、 验证半加器与全加器的逻辑功能。

3、学习二进制数的运算规律。

二、实验仪器及材料

1、仪器设备：具有 USB 接口的微型计算机一台、Altera\_FPGA 实验板、USB-Blaster 下载器一

台。

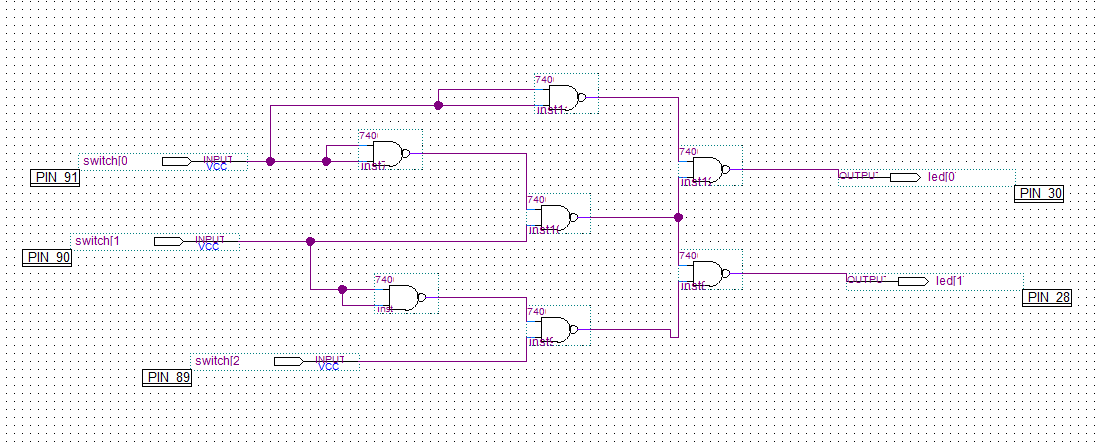
2、软件：Quartus II 13.0 以上 Altera\_FPGA 开发环境。

3、集成芯片：

74LS00 二输入端四“与非”门

74LS54 3-2-2-3 输入“与或非”门

74LS86 二输入端四“异或”门

三、实验内容

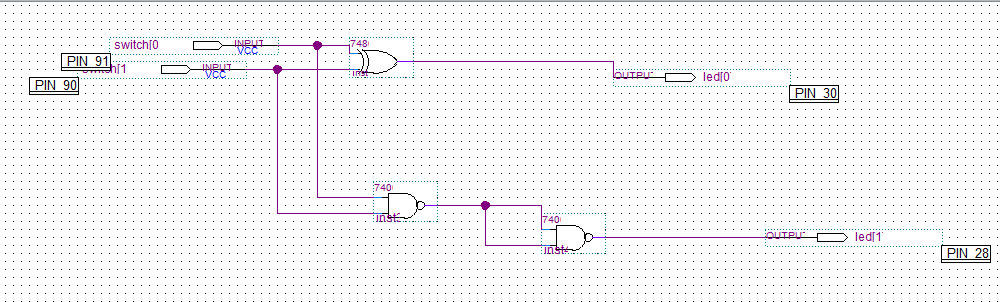
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 输入 | | | 输出 | |
| A | B | C | Y1 | Y2 |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 |





运算结果和实验完全一致

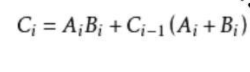
2.

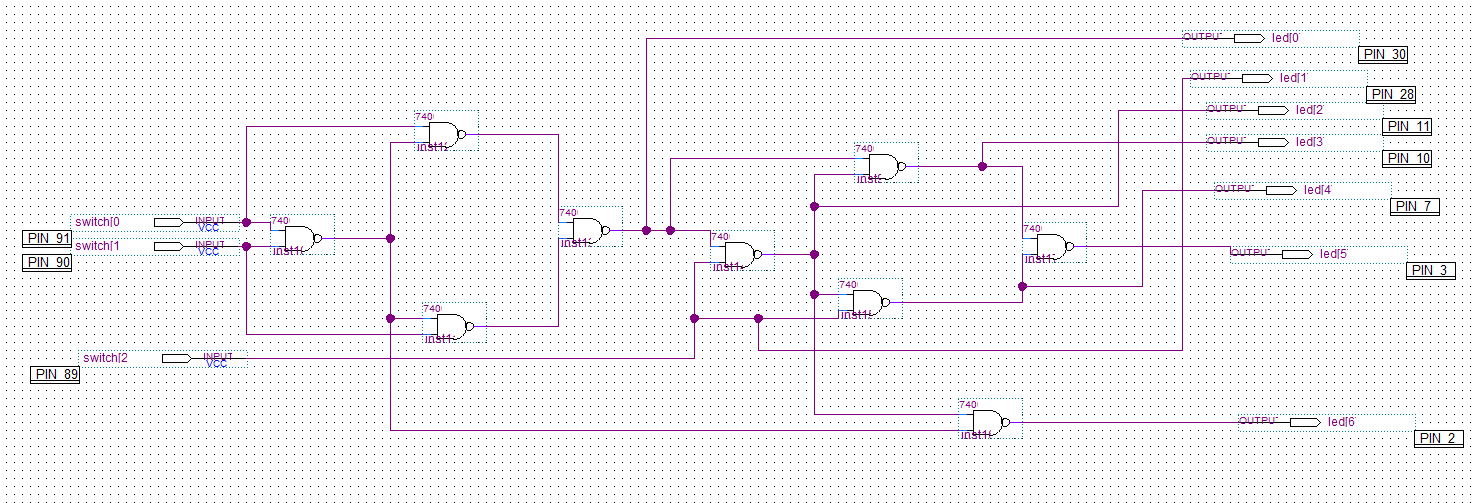


|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 输入 | A | 0 | 1 | 1 | 0 |
| B | 0 | 0 | 1 | 1 |
| 输出 | Y | 0 | 1 | 0 | 1 |
| Z | 0 | 0 | 1 | 0 |

3.







Si卡诺图

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 |

Ci卡诺图

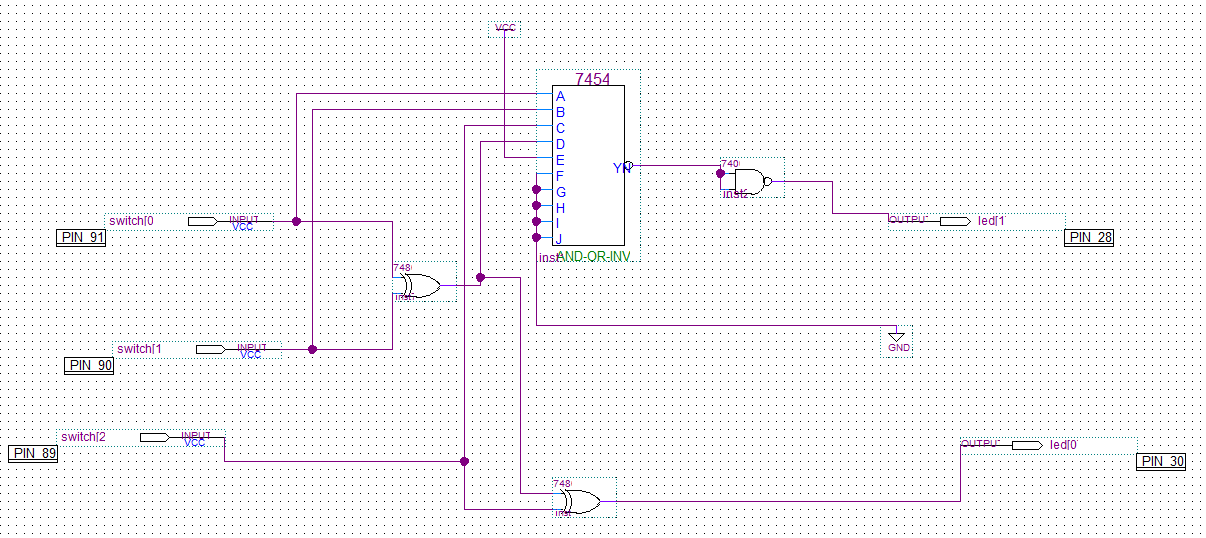
|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Ai | Bi | Ci-1 | Y | Z | X1 | X2 | X3 | SI | CI |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AI | BI | CI-1 | CI | SI |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |

逻辑功能完全一致

4.



|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 输入端 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 输出端 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |

五、实验小结

学会了如何使用组合逻辑电路，可以用真值表，卡诺图分析，并写出逻辑表达式。学习了集成芯片，减少了器件的使用，可以使用少量的几种集成芯片，更灵活地设计更多的功能。制作全加器，也让我明白了计算机是如何进行加法操作。